

U. S. Appln. No. 09/992,416

July 7, 2003

Amendment and Response to Restriction RequirementPage 2

Please replace the paragraph beginning at page 1, line 20 with the following paragraph:

AI Referring to Fig. 1, the conventional ESD protection circuit in US patent no. 5,465,189 uses a lateral semiconductor control rectifier (LSCR) and a MOS transistor to achieve ESD protection. As shown in Fig. 1, the ESD protection circuit comprises a p-substrate 16, an N-well 18, a p-type doped region 20 in the N-well 18 as an anode, and an NMOS 22. The NMOS 22 comprises a gate 26, an n-type second doped region 30 and an n-type first doped region 28. The anode 20, the N-well 18, the P-substrate 16 and the second doped region 30 form the LSCR. The first doped region 28 is formed at the junction between the N-well 18 and the P-substrate 16 to dissipate the current in the N-well 18. A p+ first contact region 34 and an n+ second contact region 36 are respectively formed in the P-substrate 16 and the N-well 18 as shown in Fig. 1. The second contact region 36 and the anode 20 are both coupled to a pad 12, then coupled to a core circuit. The gate 26 of the MOS 22 and the first contact region 34 are coupled to a power pad, such as Vss.